6. (Currently Amended) Amplifier circuit as claimed in claim 1 or claim 2 ~~one of the preceding claims~~, characterized in that it includes ~~as~~ at least one resistor (R5) mounted in parallel with the biasing cell (200).

7. (Currently Amended) Amplifier circuit as claimed in claim 1 or claim 2 ~~one of the preceding claims~~, characterized in that it includes at least one resistor (R6) mounted in series with the biasing cell (200).

8. (Currently Amended) Amplifier circuit as claimed in claim 1 or claim 2 ~~one of the preceding claims~~, characterized in that it includes an inductor (L7) and a resistor (R7) arranged in parallel, mounted in series with the biasing cell (200).

9. (Currently Amended) Amplifier circuit as claimed in claim 1 or claim 2 ~~one of the preceding claims~~, characterized in that it includes at least one resistor (R8) and one capacitor (C8) arranged in series, connected between the drain (D2) of the transistor (T2) and the ground.

10. (Original) Biasing cell (200) for amplifier circuit, characterized in that it includes at least one transistor (T2) designed to be connected between a power supply (V_{DD}) and a drain line of an amplification cell (100), characterized in that the grid (G2) of the transistor (T2) of the biasing cell (200) ~~(20)~~ is connected to the node (201) of a divider bridge (R1R2, R1T3) so as to set its grid (G2) potential (V_{G2}), and in that the grid (G2) and the source (S2) of said transistor (T2) are connected together by means of at least one capacitor (C1, C2).

NW 1/7/05